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(54) Title: Semiconductor integrated circuit and manufacturing method thereof

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Claims

1. A semiconductor integrated circuit characterized by having an insulating film, which is selectively formed on the surface of a semiconductor substrate and that divides the rest of the surface of the semiconductor substrate into multiple island regions; along with a second insulating film, which is formed on the bottom of the aforementioned island regions and is connected to the aforementioned insulating film.

2. The semiconductor integrated circuit described in Claim 1, characterized by the fact that MOSFET is formed in the aforementioned island regions.

3. A semiconductor integrated circuit manufacturing method, characterized by having the following steps:

(A) a semiconductor substrate, which has a semiconductor layer of a first electroconductivity type and another semiconductor layer of a first electroconductivity type and having a high impurity density on the first semiconductor layer, is prepared; a semiconductor layer of a second electroconductivity type is formed on the semiconductor layer of the first electroconductivity type and having a high impurity density;

(B) a second semiconductor region of the first electroconductivity type and having a high impurity density, which reaches the semiconductor layer of the first electroconductivity and having a high impurity density, is selectively formed on the aforementioned semiconductor layer of the second electroconductivity type; as a result, the aforementioned semiconductor layer of the second electroconductivity is divided into multiple island regions;

(C) by performing a [illegible; anode chemical] processing on the aforementioned semiconductor substrate, only the aforementioned semiconductor layer of the first electroconductivity type and having a high impurity density, and the second semiconductor region of the first electroconductivity type and having a high impurity density, are converted into a porous structure;

(D) the aforementioned porous semiconductor region and semiconductor layer of the first electroconductivity type are converted into insulating films;

(E) a desired semiconductor circuit element is formed in the aforementioned island regions.

4. The semiconductor integrated circuit manufacturing method described in Claim 3, characterized by the fact that in said step (A), the semiconductor layer of the second electroconductivity type is formed by epitaxial growth.

Detailed explanation of the invention

The present invention pertains to a semiconductor integrated circuit having an insulating film separation structure, and to its manufacturing method.

The electric separation methods between elements used for the semiconductor integrated circuit (referred to as IC hereinafter) are roughly classified into (1) the PN junction separation method and (2) the insulating film separation method. Since the insulating film separation method has more advantages than the other method, it will be used widely in the future. The insulating film separating structure is generally known as LOOS (local oxidation of silicon). Figure 1 shows an insulating film separating structure, which is a MOSIC structure. (1) represents an n-type region. (2), (3) represent a pair of p+ type regions used as the source region and drain region selectively formed in the n-type region (1). (4) represents a gate insulated film made of SiO_2, etc., and is formed at the position where the gate is to be formed between said p+ type regions (2), (3). (5) represents polysilicon formed on gate insulated film (4). (6) represents an insulating film made of SiO_2, etc., used for separating the elements. (7) represents a glass film that covers said polysilicon (5) and insulating film (6). (8), (9) represent the source electrode and the gate electrode formed in said p+ type regions (2), (3), respectively.

In the MOSIC with the aforementioned structure, although the ends of PN junction (10) between n-type region (1) and p+ type regions (2), (3) are separated by said insulating film (6), the line of PN junction (10) still exists in the rest of the structure. As a result, the electric separation is incomplete.

Consequently, a PN junction capacitance exists in source region (2) and drain region (3). Also, there is a parasitic capacitance caused by the wiring formed on insulating film (6) or glass film (7). The operation speed of the circuit becomes low. Also, the circuit configuration becomes complicated in order to eliminate the influence of these capacitances.

The purpose of the present invention is to solve the aforementioned problems by providing a semiconductor integrated circuit, which has an insulating film formed not only on the side ends of the semiconductor island regions where the semiconductor circuit elements are to be formed, but also on the bottom of those island regions, and by providing the manufacturing method of such a semiconductor integrated circuit.

In the following, an application example of the present invention will be explained with reference to figures. Figure 2 is a cross-sectional view illustrating the semiconductor integrated circuit disclosed in the present invention. The same parts as those shown in Figure 1 are represented by the same symbols, respectively. (11) represents a p-type semiconductor layer.

(6) represents an insulating film, which is selectively formed on the surface of the p-type semiconductor layer and divides the rest of the semiconductor layer into multiple island regions. (6') represents a second insulating film formed at the bottom of said island regions (12) and is connected to said insulating film (6). A MOSFET having, for example, p+ type source region (2) and drain region (3) as well as polysilicon gate (5) is formed in said island regions (12).

The semiconductor integrated circuit with the aforementioned configuration is manufactured using the method shown in Figure 3.

In the following, the manufacturing process will be explained with reference to Figure 3.

Step (a): As shown in Figure 3(a), boron is diffused into the surface of p-type silicon substrate (11) to form a p+ type layer (13) with a high impurity density. Then, an n-type layer (14) with the desired resistivity and thickness is formed by means of epitaxial growth on the surface of p+ type layer (13).

Step (b): As shown in Figure 3(b), boron is diffused using the conventional selectively diffusing method in said n-type layer (14) to form the second p+ type region (15) with a high impurity density that reaches said p+ type layer (13). In this way, said n-type layer (14) is divided into multiple island regions (12) by p+ type region (15).

Step (c): As shown in Figure 3(c), a [illegible, anode chemical] processing is conducted by immersing the aforementioned semiconductor substrate in, for example, hydrofluoric acid (HF). As a result, the [illegible, anode chemical] current only flows in said p+ type layer (13) and region (15), which are converted to porous silicon parts (13') and (15'), respectively.

Step (d): As shown in Figure 3(d), by performing a thermal oxidation on the aforementioned semiconductor substrate, said porous silicon parts (13') and (15') are converted into silicon oxide films (6) and (6'). Since the porous parts are oxidized more quickly than the monocrystalline silicon part in the thermal oxidation processing, silicon oxide films (6) and (6') can be formed in a short period of time.

In this way, said multiple island regions (12) are electrically separated from each other by insulating films (6) and (6').

Step (e): As shown in Figure 3(e), the conventional MOS process is used to form a MOSFET with p+ type source region (2) and drain region (3) as well as polysilicon gate (5) in island regions (12). As a result, the MOSIC with the structure shown in Figure 2 is obtained.

In the structure of the semiconductor integrated circuit disclosed in the present invention, since not only do the side ends of island regions (12), where MOSFET or other circuit elements are to be formed, but also the bottoms of these parts, are insulated and separated by insulating film (6'), the PN junction (10) does not exist as in the conventional structure. Consequently, the PN capacitance in the source region and the drain region is reduced significantly. Also, since

wiring is formed on the insulating film with its thickness increased, the parasitic capacitance is also reduced.

As explained above, according to the present invention, since insulating films are formed not only on the side ends but also at the bottoms of the semiconductor regions, where the semiconductor circuit elements are to be formed, various undesired capacitances can be suppressed. Therefore, the operation speed of the circuit can be increased.

Also, since the electric separation between the elements is improved, the circuit configuration can also be simplified.

In addition, since the area of the island regions or the insulating film regions can be reduced, a higher degree of integration can be achieved. Also, accompanying the increase in the integration degree, circuit elements with various characteristics can be formed on the same semiconductor substrate. Consequently, various types of ICs can be manufactured.

This application example explains a case of manufacturing MOSIC. However, it is also possible to apply the present invention to the case of manufacturing a bipolar IC.

Brief description of the figures

Figure 1 is a cross-sectional view illustrating a conventional example. Figure 2 and Figures 3(a)-(e) are cross-sectional views illustrating an application example of the present invention.

2 Source region
3 Drain region
5 Polysilicon gate
6, 6' Insulating films
12 Island region

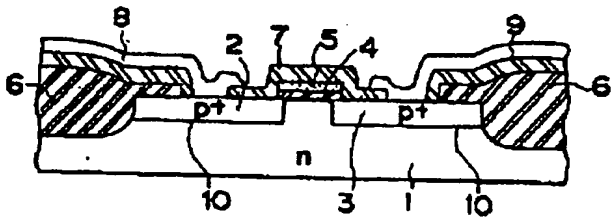

Figure 1

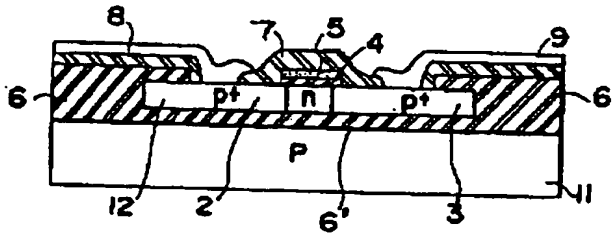

Figure 2

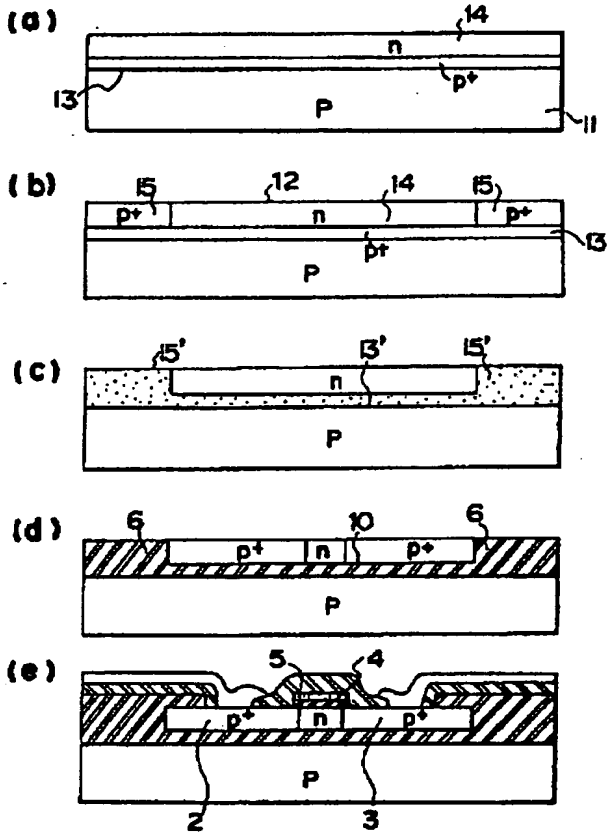

Figure 3

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Semiconductor integrated circuit and manufacturing method thereof

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